WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a memory cell array;

a chip enable transition detection circuit which detects transition of a chip enable signal that indicates a start of an operation of the memory cell array;

a first address transition detection circuit which detects transition of a row address signal that indicates a row address of the memory cell array and transition of a column address signal that indicates a column address;

a write enable transition detection circuit which detects transition of a write enable signal that indicates a write operation of the memory cell array;

a first control circuit comprising a timeout circuit which generates a control signal that controls row access of the memory cell array on the basis of detection results of the chip enable transition detection circuit, the first address transition detection circuit, and the write enable transition detection circuit;

a second address transition detection circuit which detects only the transition of the column address signal;

a second control circuit which controls column

access of the memory cell array on the basis of a detection result of the second address transition detection circuit; and

a mode determination circuit which determines a start of a mode in which column access is executed and generates a mode determination signal when a condition that allows a start of a column access operation of the memory cell array is satisfied, and the second address transition detection circuit detects the transition of the column address, or determines an end of column access and sets a standby state when column access starts, and transition of a predetermined address or a row address is detected,

wherein when the mode determination circuit determines row access, the access operation of the memory cell array is controlled by the timeout circuit in the first control circuit in read and write operations for the memory cell array, and

when the mode determination circuit determines column access, an active operation is continued while stopping control by the timeout circuit until column access is ended in the read and write operations for the memory cell array.

2. The device according to claim 1, wherein the column access operation of the memory cell array is started after a start of a sense operation for the memory cell array, and determination is executed by the

mode determination circuit on the basis of a sense amplifier enable signal output from a sense amplifier control circuit controlled by the first control circuit.

3. The device according to claim 1, which further comprises a latch circuit which, when the start of the write operation for the memory cell array is instructed after a start of a precharge operation of a word line or a plate line in a period in which the write operation is inhibited, latches write data externally input during the period in which the write operation is inhibited,

a first circuit to prolong a write mode until the write operation is enabled in a next cycle, and

a second circuit which waits for an end of the cycle and automatically starts the next cycle, and

in which the data latched by the latch circuit during the period in which the write operation is inhibited is written in a memory cell when the write operation is enabled in the next cycle, and

when the mode determination circuit determines in the next cycle the mode in which column access is executed, an active operation is continued until column access is ended.

4. The device according to claim 1, which further comprises a first latch circuit for lower bits, which, when the start of the write operation for the memory

cell array is instructed after a start of a precharge operation of a word line or a plate line in a period in which the write operation is inhibited, latches write data externally input during the period in which the write operation is inhibited,

a second latch circuit for upper bits, which, when the start of the write operation for the memory cell array is instructed after the start of the precharge operation of the word line or the plate line in the period in which the write operation is inhibited, latches write data externally input during the period in which the write operation is inhibited,

a first circuit for the lower bits to prolong a write mode until the write operation is enabled in a next cycle,

a second circuit for the upper bits to prolong the write mode until the write operation is enabled in the next cycle,

a third circuit for the low bits, which waits for an end of the cycle and automatically starts the next cycle, and

a fourth circuit for the upper bits, which waits for the end of the cycle and automatically starts the next cycle, and

in which the data latched by one of the first and second latch circuits during the period in which the write operation is inhibited is written in a memory

cell when the write operation is enabled in the next cycle, and

when the mode determination circuit determines in the next cycle the mode in which column access is executed, an active operation is continued until column access is ended.

5. The device according to claim 1, further comprising a fifth circuit which uses a row address for determination of an end of column access, and when the row address signal in a next cycle has no change, waits for an end of the cycle by the timeout circuit which generates the control signal that controls row access of the memory cell array and automatically starts the next cycle.

6. The device according to claim 1, wherein the memory cell array is formed by arraying ferroelectric cells in a matrix.

7. The device according to claim 1, wherein the memory cell array is formed by arraying TC parallel unit series-connected ferroelectric cells in a matrix.

8. The device according to claim 1, wherein the memory cell array is formed by arraying dynamic cells in a matrix.

9. A semiconductor integrated circuit device comprising:

a memory cell array;

a chip enable transition detection circuit which

detects transition of a chip enable signal that indicates a start of an operation of the memory cell array;

a first address transition detection circuit which detects transition of a row address signal that indicates a row address of the memory cell array and transition of a column address signal that indicates a column address;

a write enable transition detection circuit which detects transition of a write enable signal that indicates a write operation of the memory cell array;

a first control circuit comprising a timeout circuit which generates a control signal that controls row access of the memory cell array on the basis of detection results of the chip enable transition detection circuit, the first address transition detection circuit, and the write enable transition detection circuit;

a second address transition detection circuit which detects only the transition of the column address signal;

a second control circuit which controls column access of the memory cell array on the basis of a detection result of the second address transition detection circuit; and

a mode determination circuit which determines a start of a mode in which column access is executed and

generates a mode determination signal when a condition that allows a start of a column access operation of the memory cell array is satisfied, and the second address transition detection circuit detects the transition of the column address, or determines an end of column access and sets a standby state when column access starts, and transition of a predetermined address or a row address is detected,

wherein when the mode determination circuit determines row access, the access operation of the memory cell array is controlled by the timeout circuit in the first control circuit in read and write operations for the memory cell array,

in the write operation for the memory cell array, when the write enable transition detection circuit detects the transition of an end of the write enable signal before a period indicated by the timeout circuit, the access operation of the memory cell array is controlled by the timeout circuit,

in the write operation for the memory cell array, when the write enable transition detection circuit detects the transition of the end of the write enable signal after the period indicated by the timeout circuit, the access operation of the memory cell array is controlled in response to the transition of the write enable signal,

when the mode determination circuit determines

column access, an active operation is continued while stopping control by the timeout circuit until column access is ended in the read operation for the memory cell array, and

in the write operation for the memory cell array, the active operation is continued while stopping control by the timeout circuit or control that responds to the transition of the write enable signal until column access is ended.

10. The device according to claim 9, wherein the column access operation of the memory cell array is started after a start of a sense operation for the memory cell array, and determination is executed by the mode determination circuit on the basis of a sense amplifier enable signal output from a sense amplifier control circuit controlled by the first control circuit.

11. The device according to claim 9, which further comprises a latch circuit which, when the start of the write operation for the memory cell array is instructed after a start of a precharge operation of a word line or a plate line in a period in which the write operation is inhibited, latches write data externally input during the period in which the write operation is inhibited,

a first circuit to prolong a write mode until the write operation is enabled in a next cycle, and

a second circuit which waits for an end of the cycle and automatically starts the next cycle, and

in which the data latched by the latch circuit during the period in which the write operation is inhibited is written in a memory cell when the write operation is enabled in the next cycle, and

when the mode determination circuit determines in the next cycle the mode in which column access is executed, an active operation is continued until column access is ended.

12. The device according to claim 9, which further comprises a first latch circuit for lower bits, which, when the start of the write operation for the memory cell array is instructed after a start of a precharge operation of a word line or a plate line in a period in which the write operation is inhibited, latches write data externally input during the period in which the write operation is inhibited,

a second latch circuit for upper bits, which, when the start of the write operation for the memory cell array is instructed after the start of the precharge operation of the word line or the plate line in the period in which the write operation is inhibited, latches write data externally input during the period in which the write operation is inhibited,

a first circuit for the lower bits to prolong a write mode until the write operation is enabled in a

next cycle,

a second circuit for the upper bits to prolong the write mode until the write operation is enabled in the next cycle,

a third circuit for the low bits, which waits for an end of the cycle and automatically starts the next cycle, and

a fourth circuit for the upper bits, which waits for the end of the cycle and automatically starts the next cycle, and

in which the data latched by one of the first and second latch circuits during the period in which the write operation is inhibited is written in a memory cell when the write operation is enabled in the next cycle, and

when the mode determination circuit determines in the next cycle the mode in which column access is executed, an active operation is continued until column access is ended.

13. The device according to claim 9, further comprising a fifth circuit which uses a row address for determination of an end of column access, and when the row address signal in a next cycle has no change, waits for an end of the cycle by the timeout circuit which generates the control signal that controls row access of the memory cell array and automatically starts the next cycle.

14. The device according to claim 9, wherein the memory cell array is formed by arraying ferroelectric cells in a matrix.

15. The device according to claim 9, wherein the memory cell array is formed by arraying TC parallel unit series-connected ferroelectric cells in a matrix.

16. The device according to claim 9, wherein the memory cell array is formed by arraying dynamic cells in a matrix.